211134US-2S

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :

FUMIO HIRAHARA ET AL : EXAMINER: MITCHELL, J.

SERIAL NO: 09/900,946 :

FILED: JULY 10, 2001 : GROUP ART UNIT: 2827

FOR: SEMICONDUCTOR DEVICE HAVING AT LEAST THREE POWER TERMINALS SUPERPOSED ON EACH OTHER

#7/A
Amdt
J. Mitchell
7/30/02

AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

In response to the Official Action mailed April 24, 2002, please amend this application as follows:

IN THE CLAIMS

Please amend Claims 1-10 to read as follows:[1]

1. (Amended) A semiconductor device comprising:

A1

at least three power terminals provided one above the other; and

at least one semiconductor chip having an upper surface and a lower surface and interposed between a predetermined two power terminals of said at least three power

[1]A marked-up copy of the claims is attached.

terminals with the upper and lower surfaces of the at least one semiconductor chip electrically connected to the two power terminals.

2. (Amended) The semiconductor device according to claim 1, wherein the uppermost one and lowermost one of said at least three power terminals extend in the same direction.

3. (Amended) The semiconductor device according to claim 2, wherein a power terminal positioned at the middle among said at least three power terminals extends in a direction opposite to or perpendicular to the uppermost one or lowermost one of said at least three power terminals.

Cont'd A1

4. (Amended) The semiconductor device according to claim 1, wherein one face of said at least one semiconductor chip interposed between said two power terminals is connected to one power terminal of said two power terminals by soldering or pressure welding, and another face is connected to another power terminal of said two power terminals by soldering or pressure welding through a buffer plate.

5. (Amended) The semiconductor device according to claim 1, wherein two currents flow in opposite directions in said uppermost one and lowermost one of said at least three power terminals, while said at least one semiconductor chip is operating.

6. (Amended) The semiconductor device according to claim 1, wherein said at least one semiconductor chip interposed between said two power terminals includes a plurality of semiconductor chips, and at least one insulation layer is provided between said plurality of semiconductor chips.

7. (Amended) The semiconductor device according to claim 6, wherein said plurality of semiconductor chips includes at least one transistor and at least one diode, and wherein at

least one control electrode is connected to said at least one transistor to control said at least one transistor.

8. (Amended) The semiconductor device according to claim 7, wherein said at least one transistor has a control electrode pad, said control electrode is connected to said control electrode pad by wire bonding or by interposing a buffer plate between said control electrode and said control electrode pad.

9. (Amended) The semiconductor device according to claim 7, wherein said control electrode is led out in a direction opposite to or perpendicular to the uppermost one or lowermost one of said at least three power terminals.

Cont'd A1

10. (Amended) The semiconductor device according to claim 4, wherein the uppermost one and lowermost one of said at least three power terminals have a screw fixing structure so as to connect said at least one semiconductor chip by pressure welding between said two power terminals.

Please add new Claims 11-19 as follows:

11. (New) A semiconductor device comprising:

at least three power terminals provided one above another; and

A2

at least one semiconductor chip having an upper surface and a lower surface and interposed between a predetermined two power terminals of said at least three power terminals, with the upper and lower surfaces of the at least one semiconductor chip electrically connected to the two power terminals,

wherein one face of said at least one semiconductor chip interposed between said two power terminals is connected to one power terminal of said two power terminals by soldering or pressure welding, and another face is connected to another power terminal of said two power terminals by soldering or pressure welding.

12. (New) The semiconductor device according to claim 11, wherein the uppermost one and lowermost one of said at least three power terminals extend in the same direction.

13. (New) The semiconductor device according to claim 12, wherein a power terminal positioned at the middle among said at least three power terminals extends in a direction opposite to or perpendicular to the uppermost one or lowermost one of said at least three power terminals.

14. (New) The semiconductor device according to claim 11, wherein two currents flow in opposite directions in said uppermost one and lowermost one of said at least three power terminals, while said at least one semiconductor chip is operating.

Cont'd A2

15. (New) The semiconductor device according to claim 11, wherein said at least one semiconductor chip interposed between said two power terminals includes a plurality of semiconductor chips, and at least one insulation layer is provided between said plurality of semiconductor chips.

16. (New) The semiconductor device according to claim 15, wherein said plurality of semiconductor chips includes at least one transistor and at least one diode, and wherein at least one control electrode is connected to said at least one transistor to control said at least one transistor.

17. (New) The semiconductor device according to claim 16, wherein said at least one transistor has a control electrode pad, said control electrode is connected to said control electrode pad by wire bonding or by interposing a buffer plate between said control electrode and said control electrode pad.

18. (New) The semiconductor device according to claim 16, wherein said control electrode is led out in a direction opposite to or perpendicular to the uppermost one or lowermost one of said at least three power terminals.

19. (New) The semiconductor device according to claim 11, wherein the uppermost one and lowermost one of said at least three power terminals have a screw fixing structure so as to connect said at least one semiconductor chip by pressure welding between said two power terminals.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-19 are pending in the present application. Claims 1-10 have been amended and Claims 11-19 have been added by the present amendment.

In the outstanding Office Action, Claims 2, 3, 5 and 7-10 were rejected under 35 U.S.C. § 112, second paragraph; Claims 1-4 and 6-8 were rejected under 35 U.S.C. § 102(b) as anticipated by Matsuda; and Claims 9-10 were indicated as allowable if rewritten in independent form.

Applicants thank the Examiner for the indication of allowable subject matter.

Regarding the rejection of Claims 2, 3, 5 and 7-10 under 35 U.S.C. § 112, second paragraph, the appropriate claims have been amended in light of the comments noted in the outstanding Office Action and as shown in the marked-up copy. Further, regarding Claim 5, the outstanding Office Action indicates it is ambiguous as to whether a current in the opposite direction is equivalent to a reverse bias and if not, what characteristics distinguish a current in an opposite direction. Applicants note Claim 5 has been amended to recite that two currents flow in opposite directions in the uppermost one end and lowermost one of the at least three power terminals while the at least one semiconductor chip is operating as shown

in Figure 1B, for example. Accordingly, it is respectfully requested this rejection be withdrawn.

Claims 1-4 and 6-8 stand rejected under 35 U.S.C. § 102(b) as anticipated by Matsuda. This rejection is respectfully traversed.

The present invention as recited in Claim 1 is directed to a semiconductor device including at least three power terminals provided one above another, and at least one semiconductor chip having an upper surface and a lower surface. The semiconductor chip is interposed between two power terminals of the at least three power terminals with the upper and lower surfaces of the semiconductor chip being electrically connected to the two power terminals.

For example, as shown in Figures 1A and 1B, the semiconductor device includes at least three power terminals 3, 8, 4 provided one above another, and at least one semiconductor chip 11 having an upper surface and a lower surface and interposed between two power terminals with the upper and lower surfaces being electrically connected to the two power terminals.

The outstanding Office Action states Matsuda teaches the claimed invention and cites Figure 1. However, Applicants note Figure 1 clearly illustrates that the power terminals 3, 5, 7 are adjacently arranged in parallel and are not arranged one above another as recited in Claim 1 of the present invention. In addition, the lower surfaces of the semiconductor chips (i.e., transistor 29 and diode 31) are arranged on top of the second conductor (Cu layer 15), and the upper surfaces of the semiconductor chips (transistor 29 and diode 31) are connected to the Cu layer 25 by the aluminum bonding wire 33. Thus, Matsuda does not teach or suggest a structure in which the upper and lower surfaces of a semiconductor chip are

interposed between a predetermined two power terminals of at least three power terminals and are connected to the two power terminals as claimed by the present invention.

Therefore, it is respectfully submitted independent Claim 1 and each of the claims depending therefrom are allowable.

In addition, new Claims 11-19 have been added to set forth the invention in a varying scope, and Applicants submit the new claims are supported by the originally-filed specification. It is respectfully submitted these claims are also allowable for similar reasons as Claims 1-10.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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